WHAT IS CLAIMED IS:

1. A MOSgated semiconductor device comprising:

a channel receiving region of a first conductivity type;

a channel region of a second conductivity type formed in said channel receiving region;

a plurality of spaced trenches formed in said channel receiving region;

a first region of a first conductivity type formed at the bottom of each trench, each said first region of said first conductivity type being adjacent to said channel receiving region and of a higher conductivity than said channel receiving region;

a plurality of conductive regions of said first conductivity type each disposed adjacent a trench; and

a contact layer formed over said channel receiving region and in ohmic contact with said plurality of contact regions.

2. A device according to claim 1, further comprising field relief regions of said second conductivity type formed below said channel region.

3. A device according to claim 2, wherein said field relief regions are spaced from said channel region.

4. A device according to claim 1, wherein said channel receiving region is an epitaxial layer of semiconductive material formed over a substrate.

5. A device according to claim 4, further comprising a second contact formed over said substrate.

6. A device according to claim 5, wherein said second contact is a trimetal contact.

7. A device according to claim 1, further comprising high conductivity contact regions of said second conductivity type formed in said channel region and in ohmic contact with said contact layer.

8. A device according to claim 1, wherein said conductive regions are source regions.

9. A device according to claim 1, wherein each of said trenches is filled with a conductive material and lined at each side wall thereof with a gate insulation material.

10. A MOSgated semiconductor device comprising:

a semiconductor die having an epitaxial layer of a first conductivity type formed over a substrate;

a channel region of a second conductivity type formed in said epitaxial layer;

a plurality of spaced trenches formed in said epitaxial layer;

a first region of a first conductivity type formed at the bottom of each trench, each said first region of said first conductivity type being adjacent to said epitaxial layer and of a higher conductivity than said epitaxial layer;

a plurality of source regions of said first conductivity type each disposed adjacent a trench; and

a source contact formed over said epitaxial layer and in ohmic contact with said plurality of contact regions.

11. A device according to claim 10, further comprising field relief regions of said second conductivity type formed below said channel region.

12. A device according to claim 11, wherein said field relief regions are spaced from said channel region.

13. A device according to claim 10, wherein said substrate is a semiconductive material of the same conductivity type as said epitaxial layer but of lower conductivity.

14. A device according to claim 13, further comprising a drain contact formed over said substrate.

15. A device according to claim 14, wherein said second contact is a trimetal contact.

16. A device according to claim 10, further comprising high conductivity contact regions of said second conductivity type formed in said channel region and in ohmic contact with said source contact.

17. A device according to claim 10, wherein each of said trenches is filled with a conductive material and lined at each side wall thereof with a gate insulation material.

18. A device according to claim 17, wherein said conductive material is polysilicon and said gate insulation material is oxide.

19. A device according to claim 1, wherein said trenches extend to a depth below said channel region.

20. A device according to claim 17, wherein said trenches extend to a depth below said channel region.